Roll No. | | | | | | | | | | |

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E / B. Tech (Full Time) END SEMESTER EXAMINATIONS – APRIL/MAY 2025

ELECTRICAL & ELECTRONICS ENGINEERING
Fourth semester
EE 5401 Digital Electronics
(Regulation 2019)

Time: 3 Hours | Answer ALL Questions | Max. Marks 100

PART- A (10 x 2 = 20 Marks)

Q.No	Questions	Marks
1.	What happens when both inputs are given as '0', in an S-R latch implemented using two number of 2-input NAND gates.	2
2.	What is 'Toggle flip-flop' ? Given a JK flip-flop, is it possible to achieve a toggle flip-flop?	2
3.	Subtract 1001_2 from 1010_2 using 2's complement method. Also verify your answer by directly subtracting.	2
4.	State anyone of the DeMorgan's theorems.	2
5.	What is a parity checker?	2
6.	To implement a full adder, how many half-adders are required? Apart from these half-adders what gate(s) is/are required? Show the circuitry.	2
7.	Distinguish between PAL and PLA.	2
8.	How will you realize a 2-input XOR gate, using only NAND gates?	2
9.	Draw a circuit diagram showing how a NOR gate is realized in CMOS family?	2
10.	What do you understand from 'register transfer language'?	2

PART- B (5 x 13 = 65 Marks)

(Restrict to a maximum of 2 subdivisions)

Q.No	Questions	Marks
11.	a) Using Karnaugh map method, minimize the function f(a,b,c,d) = $\sum m\{0,1,3,4,7,8,10,11,12,15\}$ + d{6,9} and implement using 2-input AND and 2-input OR gates apart from NOT gates. Here, d- denotes the don't care conditions	13
	OR	
	b). Using Quine McCluskey tabulation method, minimize the function f(a,b,c,d) = $\sum m\{0,1,3,4,7,10,11,12,15\}$ + d{9} and implement using only NAND gates. Here, d- denotes the don't care conditions	13
12.	a) Given one number 4-bit adder IC (7483) along with a quad XOR gate IC, how would you realize an adder / subtractor circuit? Assume that when the control bit is '0' addition is required to be performed and when the control bit is '1' subtraction is to be carried out. Discuss the operation of the circuit.	13
	OR	
	b) i) What is a 2 x 4 decoder? How can it be used as a demultiplexer with two selection lines? ii) Using a '1 – of – 4' multiplexer, realize the function f(a,b,c) = b' + a'c (5 + 8)	13
13.	a) Using T-flipflops, design a synchronous sequential counter that counts the repeating sequence: 1,5,3,6,7,again 1,5 ..,	13

OR

b) Minimize the state table: **13**

Present State	Next State, z (when x = 0)	Next State, z (when x = 1)
A	C,0	B,0
B	C,0	D,0
C	C,0	B,0
D	E,1	D,0
E	E,1	F,1
F	C,0	F,1

using, either 'partitioning method' or 'implication method'. Here, x is the single bit input and z- is the single bit output.

14. a) Obtain the merged flow table for the primitive flow table : **13**

x_1x_2 = 00	x_1x_2 = 01	x_1x_2 = 11	x_1x_2 = 10
"1"	5	6	2
1	-	-	"2"
-	5	"3"	2
"4"	5	3	-
-	5	"6"	2
4	"5"	-	-

OR

b). What is a ripple counter? Design a mod-7 asynchronous counter using JK - flip flops. **13**

15. a) i) Assuming even parity scheme, determine the Hamming code for the data bit pattern: 11010101_2. **13**
ii) Illustrate with a suitable example, how 'when – else' statement is used in VHDL description? (4 + 9)

OR

b) Give functional VHDL description/ program of a 4-to-1 multiplexer. Explain. **13**

PART- C (1 x 15 = 15 Marks)

(Q. No 16 is Compulsory)

Q.No	Questions	Marks
16.	i) Explain how XNOR gate is realized in RTL family. Also suggest an application for the XNOR gate. ii) Explain how NOT gate is implemented using a simple npn based switching transistor, and how it can be added to the circuit of previous part, in order to realize XOR gate? How is XOR gate useful in adder circuits? How is it useful as a code converter? How is it useful in parity generation? (7 + 8)	15